

**EFFICIENT ALGORITHM TO OPTIMIZE BUFFERS IN
MINTIMING FIXES**

Umesh Nair

ABSTRACT OF THE DISCLOSURE

- 5 A method for optimizing buffers in an integrated circuit design. The method includes identifying paths and nodes within the integrated circuit design, determining node overlap within the integrated circuit design, calculating possible solutions for addressing timing violations within the integrated circuit design, choosing a solution for addressing timing violations, inserting buffers at particular nodes of the integrated
10 circuit design, and repeating the calculated possible solutions wherein choosing a solution and inserting buffers at particular nodes to address timing violations are within the integrated circuit design.